

## WHAT IS CLAIMED IS:

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1	1. A method for manufacture of a MOSFET device, the method comprising:
2	providing for a semiconductor substrate;
3	providing for an electrically insulating layer in contact with the semiconductor
4	substrate, the insulating layer having a dielectric constant greater than 4.0;
5	providing for a gate electrode in contact with at least a portion of the insulating layer;
6	and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

- 2. The method of claim 1, wherein the MOSFET device is a planar P-type or N-type MOSFET, having any orientation.
- 3. The method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
  - 4. The method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 5. The method of claim 1, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 6. The method of claim 1, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
- 7. The method of claim 1, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 8. The method of claim 1, wherein dopants are introduced into the channel region.

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1	9. A method for manufacture of a MOSFET device, the method comprising:
2	providing for a semiconductor substrate;
3	providing for an electrically insulating layer in contact with the semiconductor
4	substrate, the insulating layer having a dielectric constant greater than 7.6;
5	providing for a gate electrode in contact with at least a portion of the insulating layer;
6	and
7	providing a source electrode and a drain electrode in contact with the semiconductor
8	substrate and proximal to the gate electrode wherein at least one of the source electrode and
9	the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor
10	substrate.

- 10. The method of claim 9, wherein the MOSFET device is a planar P-type or N-type MOSFET, having any orientation.
  - 11. The method of claim 9, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
  - 12. The method of claim 9, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 13. The method of claim 9, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 14. The method of claim 9, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
- 1 15. The method of claim 9, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 16. The method of claim 9, wherein dopants are introduced into the channel region.

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substrate.

1	17. A method for manufacture of a MOSFET device, the method comprising:
2	providing for a semiconductor substrate;
3	providing for an electrically insulating layer in contact with the semiconductor
4	substrate, the insulating layer having a dielectric constant greater than 15;
5	providing for a gate electrode in contact with at least a portion of the insulating layer;
6	and
7	providing a source electrode and a drain electrode in contact with the semiconductor
8	substrate and proximal to the gate electrode wherein at least one of the source electrode and

1 18. The method of claim 17, wherein the MOSFET device is a planar P-type or N-2 type MOSFET, having any orientation.

the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor

- 19. The method of claim 17, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
- 20. The method of claim 17, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 21. The method of claim 17, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 22. The method of claim 17, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
- 1 23. The method of claim 17, wherein an entire interface between at least one of 2 the source electrode and the drain electrode and the semiconductor substrate forms a 3 Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 24. The method of claim 17, wherein dopants are introduced into the channel 2 region.

1	25. A method for manufacture of a MOSFET device, the method comprising:		
2	providing for a semiconductor substrate;		
3	providing for an electrically insulating layer in contact with the semiconductor		
4	substrate, the insulating layer having a dielectric constant greater than 4.0;		
5	providing for a gate electrode located in contact with at least a portion of the		
6	insulating layer;		
7	exposing the semiconductor substrate on one or more areas proximal to the gate		
8	electrode;		
9	providing for a thin film of metal on at least a portion of the exposed semiconductor		
10	substrate; and		
11	reacting the metal with the exposed semiconductor substrate such that a Schottky or		
12	Schottky-like source electrode and drain electrode are formed on the semiconductor		
13	substrate.		
1	26. The method of claim 25, wherein the MOSFET device is a planar P-type or N		
2	type MOSFET, having any orientation.		
1	27. The method of claim 25, wherein the gate electrode is provided by:		
2	depositing a thin conducting film on the insulating layer;		
3	patterning and etching the conducting film to form a gate electrode; and		
4	forming one or more thin insulating layers on one or more sidewalls of the gate		
5	electrode.		

- 1 28. The method of claim 25, further comprising removing metal not reacted 2 during the reacting process.
  - 29. The method of claim 25, wherein the reacting comprises thermal annealing.
- 1 30. The method of claim 25, wherein the source and drain electrodes are formed 2 from a member of the group consisting of: platinum silicide, palladium silicide and iridium 3 silicide.
- 1 31. The method of claim 25, wherein the source and drain electrodes are formed 2 from a member of the group consisting of the rare earth silicides.

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1	32.	The method of claim 25, wherein the insulating layer is formed from a
2	member of the	e group consisting of metal oxides.

- 33. The method of claim 25, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.
- 1 34. The method of claim 25, wherein an entire interface between at least one of 2 the source electrode and the drain electrode and the semiconductor substrate forms a
- 3 Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 35. The method of claim 25, wherein dopants are introduced into the channel region.
  - 36. A method for manufacture of a MOSFET device, the method comprising: providing for a semiconductor substrate;
  - providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6;
  - providing for a gate electrode located in contact with at least a portion of the insulating layer;
  - exposing the semiconductor substrate on one or more areas proximal to the gate electrode;
  - providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and
- reacting the metal with the exposed semiconductor substrate such that a Schottky or

  Schottky-like source electrode and drain electrode are formed on the semiconductor

  substrate.
- 1 37. The method of claim 36, wherein the MOSFET device is a planar P-type or N-2 type MOSFET, having any orientation.
- 1 38. The method of claim 36, wherein the gate electrode is provided by:
- depositing a thin conducting film on the insulating layer;
- patterning and etching the conducting film to form a gate electrode; and
- forming one or more thin insulating layers on one or more sidewalls of the gate
- 5 electrode.

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1	39.	The method of claim 36, further comprising removing metal not reacted
2	during the rea	cting process.

- 1 40. The method of claim 36, wherein the reacting comprises thermal annealing.
- 1 41. The method of claim 36, wherein the source and drain electrodes are formed 2 from a member of the group consisting of: platinum silicide, palladium silicide and iridium 3 silicide.
- 1 42. The method of claim 36, wherein the source and drain electrodes are formed 2 from a member of the group consisting of the rare earth silicides.
  - 43. The method of claim 36, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
  - 44. The method of claim 36, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.
  - 45. The method of claim 36, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
  - 46. The method of claim 36, wherein dopants are introduced into the channel region.
- 1 47. A method for manufacture of a MOSFET device, the method comprising: 2 providing for a semiconductor substrate;
- providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;
- providing for a gate electrode located in contact with at least a portion of the insulating layer;
- exposing the semiconductor substrate on one or more areas proximal to the gate electrode;
- providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and



- reacting the metal with the exposed semiconductor substrate such that a Schottky or 11 Schottky-like source electrode and drain electrode are formed on the semiconductor 12 13 substrate.
- 48. The method of claim 47, wherein the MOSFET device is a planar P-type or N-1 type MOSFET, having any orientation. 2
- 49. The method of claim 47, wherein the gate electrode is provided by: 1 depositing a thin conducting film on the insulating layer; 2
- patterning and etching the conducting film to form a gate electrode; and 3 forming one or more thin insulating layers on one or more sidewalls of the gate 4 5 electrode.
- 50. The method of claim 47, further comprising removing metal not reacted 1 2 during the reacting process.
- 51. The method of claim 47, wherein the reacting comprises thermal annealing. 1
- 52. The method of claim 47, wherein the source and drain electrodes are formed 1 from a member of the group consisting of: platinum silicide, palladium silicide and iridium 2 silicide. 3
  - 53. The method of claim 47, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 54. The method of claim 47, wherein the insulating layer is formed from a 1 member of the group consisting of metal oxides. 2
- 55. The method of claim 47, wherein the Schottky contact or Schottky-like region 1 2 is formed at least in areas adjacent to the channel.
- 56. The method of claim 47, wherein an entire interface between at least one of 1 2 the source electrode and the drain electrode and the semiconductor substrate forms a
- Schottky contact or Schottky-like region with the semiconductor substrate. 3

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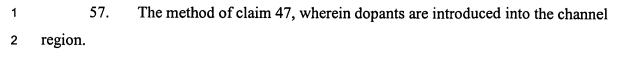
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- 58. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
- 3 providing for a semiconductor substrate;
- providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0;
- providing for a gate electrode in contact with at least a portion of the insulating layer;

  and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

- 59. The method of claim 58, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
- 60. The method of claim 58, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 61. The method of claim 58, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 62. The method of claim 58, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.
- 1 63. The method of claim 58, wherein an entire interface between at least one of 2 the source electrode and the drain electrode and the semiconductor substrate forms a 3 Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 64. The method of claim 58, wherein dopants are introduced into the channel region.

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1	65.	A method for manufacture of a device for regulating the flow of electrical
2	current, the m	nethod comprising:
3	provi	ding for a semiconductor substrate;
4	provi	ding for an electrically insulating layer in contact with the semiconductor
5	substrate, the	insulating layer having a dielectric constant greater than 7.6;
6	provid	ding for a gate electrode in contact with at least a portion of the insulating layer;
7	and	
8	provi	ding a source electrode and a drain electrode in contact with the semiconductor
9	substrate and	proximal to the gate electrode wherein at least one of the source electrode and
10	the drain elec	ctrode forms a Schottky contact or Schottky-like region with the semiconductor
11	substrate.	

- 66. The method of claim 65, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
- 67. The method of claim 65, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 68. The method of claim 65, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 69. The method of claim 65, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
  - 70. The method of claim 65, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- The method of claim 65, wherein dopants are introduced into the channel region.
- 1 72. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
- 3 providing for a semiconductor substrate;

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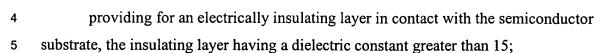
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providing for a gate electrode in contact with at least a portion of the insulating layer;

and

providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate.

- 73. The method of claim 72, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
- The method of claim 72, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- The method of claim 72, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
  - 76. The method of claim 72, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel.
- The method of claim 72, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- The method of claim 72, wherein dopants are introduced into the channel region.
- 1 79. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
- providing for a semiconductor substrate;
- providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0:

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6	providing for a gate electrode located in contact with at least a portion of the	
7	insulating layer;	
8	exposing the semiconductor substrate on one or more areas proximal to the gate	
9	electrode;	
0	providing for a thin film of metal on at least a portion of the exposed semiconductor	
1	substrate; and	
2	reacting the metal with the exposed semiconductor substrate such that a Schottky or	
3	Schottky-like source electrode and drain electrode are formed on the semiconductor	
4	substrate.	
1	80. The method of claim 79, wherein the gate electrode is provided by:	

- depositing a thin conducting film on the insulating layer; patterning and etching the conducting film to form a gate electrode; and forming one or more thin insulating layers on one or more sidewalls of the gate electrode.
- 81. The method of claim 79, further comprising removing metal not reacted during the reacting process.
  - 82. The method of claim 79, wherein the reacting comprises thermal annealing.
- 83. The method of claim 79, wherein the source and drain electrodes are formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide.
- 84. The method of claim 79, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
- 85. 1 The method of claim 79, wherein the insulating layer is formed from a 2 member of the group consisting of metal oxides.
- 86. The method of claim 79, wherein the Schottky contact or Schottky-like region 1 is formed at least in areas adjacent to the channel. 2

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insulating layer;

electrode.

87.	The method of claim 79, wherein an entire interface between at least one of
the source ele	ectrode and the drain electrode and the semiconductor substrate forms a
Schottky contact or Schottky-like region with the semiconductor substrate.	
88.	The method of claim 79, wherein dopants are introduced into the channel
region.	
89.	A method for manufacture of a device for regulating the flow of electrical
current, the m	nethod comprising:
providing for a semiconductor substrate;	
provid	ling for an electrically insulating layer in contact with the semiconductor
substrate, the	insulating layer having a dielectric constant greater than 7.6;
provid	ling for a gate electrode located in contact with at least a portion of the
	the source electric substrate, the

electrode;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

exposing the semiconductor substrate on one or more areas proximal to the gate

reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate.

- 90. The method of claim 89, wherein the gate electrode is provided by:
  depositing a thin conducting film on the insulating layer;
  patterning and etching the conducting film to form a gate electrode; and
  forming one or more thin insulating layers on one or more sidewalls of the gate
- 1 91. The method of claim 89, further comprising removing metal not reacted during the reacting process.
  - 92. The method of claim 89, wherein the reacting comprises thermal annealing.

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93.	The method of claim 89, wherein the source and drain electrodes are formed
from a memb	er of the group consisting of: platinum silicide, palladium silicide and iridium
silicide.	

- 1 94. The method of claim 89, wherein the source and drain electrodes are formed 2 from a member of the group consisting of the rare earth silicides.
- 1 95. The method of claim 89, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 96. The method of claim 89, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
  - 97. The method of claim 89, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 98. The method of claim 89, wherein dopants are introduced into the channel 2 region.
  - 99. A method for manufacture of a device for regulating the flow of electrical current, the method comprising:
- 3 providing for a semiconductor substrate;
  - providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 15;
- providing for a gate electrode located in contact with at least a portion of the insulating layer;
- exposing the semiconductor substrate on one or more areas proximal to the gate electrode;
- providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and

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12	reacting the metal with the exposed semiconductor substrate such that a Schottky or
13	Schottky-like source electrode and drain electrode are formed on the semiconductor
14	substrate.

- 1 100. The method of claim 99, wherein the gate electrode is provided by:
- depositing a thin conducting film on the insulating layer;
- patterning and etching the conducting film to form a gate electrode; and
- forming one or more thin insulating layers on one or more sidewalls of the gate electrode.
- 1 101. The method of claim 99, further comprising removing metal not reacted 2 during the reacting process.
- 1 102. The method of claim 99, wherein the reacting comprises thermal annealing.
- 1 103. The method of claim 99, wherein the source and drain electrodes are formed 2 from a member of the group consisting of: platinum silicide, palladium silicide and iridium 3 silicide.
  - 104. The method of claim 99, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides.
  - 105. The method of claim 99, wherein the insulating layer is formed from a member of the group consisting of metal oxides.
- 1 106. The method of claim 99, wherein the Schottky contact or Schottky-like region 2 is formed at least in areas adjacent to the channel.
- 1 107. The method of claim 99, wherein an entire interface between at least one of
- the source electrode and the drain electrode and the semiconductor substrate forms a
- 3 Schottky contact or Schottky-like region with the semiconductor substrate.
- 1 108. The method of claim 99, wherein dopants are introduced into the channel 2 region.